วงจร CDBA แบบตัวถี่กว้าง แบบใช้แรงดันไฟฟ้า เล็กย่อม และ การนำไปประยุกต์ใช้ในวงจรของสัญญาณแสดงเครื่องแบบกระแทก

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บทคัดย่อ

บทความนี้นำเสนอการออกแบบวงจร current differencing buffered amplifier (CDBA) เพื่อ
การนำไปประยุกต์ใช้ในวงรรมประดีดสัญญาณแบบใช้แรงดันไฟฟ้า เล็กย่อม และ
วงจร CDBA ที่นำเสนอใหม่รูปแบบช่วงและสามารถทำงานได้ในแรงดันไฟฟ้าเดียวกัน düสต์ระดับ 2 โวลต์ สามารถในการทำงานของ
วงจรที่ได้รับการออกแบบได้ดีตามหลักการและแนวความรู้แบบ PSPICE นอกจากนี้
ยังมีการนำเสนอแนวการใช้ประโยชน์ในการออกแบบวงรรมประดีดสัญญาณแบบ leapfrog เพื่อส่งเสริมการใช้
วงจรของสัญญาณแสดงเครื่องแบบกระแทกความที่ถูกต้องได้

คำสำคัญ: วงจร CDBA, วงจรโหมดกระแส, วงจรตัวถี่แสดงเครื่องแบบ, วงจรแรงดันไฟฟ้าเล็กย่อม

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Low-Voltage Wide-Bandwidth CDBA and Its Application to Current-Mode Ladder Filters

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Abstract

In this paper, a design of current differencing buffered amplifier (CDBA) for low-voltage applications is presented. The proposed CDBA is simple and is designed to operate with a minimum power supply of 2 volts. The PSPICE simulation results demonstrating the circuit performance are included. Some design procedures using this CDBA as an active element in the leapfrog simulation of high frequency current-mode ladder filters are also introduced.

Keywords: Current Differencing Buffered Amplifier (CDBA), current-mode circuit, ladder filter, low-voltage circuit

Original manuscript submitted: July 14, 2004 and Final manuscript received: October 11, 2004
Introduction

During the past few years, comparing with voltage-mode techniques, current-mode signal processing techniques have been received a wide attention due to its wide bandwidth, low-voltage operation and simple implementation of signal operations such as addition and subtraction. Usually, the design of high performance current-mode circuits employ circuit building blocks such as second-generation current conveyors (CCIIs) and current feedback amplifiers (CFAs). Recently, a current differencing buffered amplifier (CDBA) has been first proposed [C. Acar and S. Ozoguz. 1999] which is particularly suitable for the current-mode operation and realization of continuous-time filters. The CDBA can offer high-slew rate, wide bandwidth and simple implementation [S. Ozoguz, A. Toker, and C. Acar. 1999]. It is beneficial to use CDBAs as a building block to realize the most general $n$th-order voltage-mode and current-mode transfer functions [C. Acar and H. Sedef. 2003.] In addition, CDBA-based circuit implementation is suitable for current-mode continuous-time fully integrated MOSFET-C filters, especially for filters using MOS resistive circuit, MRC [S. Ozoguz, A. Toker, and C. Acar. 1999], and filters that can operate at a low supply voltage. A low-voltage technique is one of the most important issues because of the advance of the large-scale integration with complicated circuit systems and the increasing demands for battery-operated portable equipments. This paper proposes a low-voltage CDBA, which can operate at a low DC power supply voltage of 2 volts. The PSPICE simulation results of the proposed low-voltage CDBA show a low power consumption and a wide bandwidth. Since the proposed circuit considerably simplifies the realization of high frequency current-mode active ladder filters, a realization of the leapfrog structure of current-mode ladder filters in which CDBA is employed as an active element is shown as an application of the CDBA. The presented method shows that the CDBA-based leapfrog simulation is simple and suitable for realizing of the current-mode ladder filters. Most importantly, the current-mode ladder filters with CDBAs employ less active components compared with CCIIs-based ladder filter implementations [E.I. El-Masry. 1996.]

Basic Principle

The representation of the CDBA is shown in Fig.1 whose current and voltage characteristics can be described by the following relations [C. Acar and S. Ozoguz. 1999 and C. Acar and H. Sedef. 2003. ]:

\[ v_p = 0, \quad v_n = 0, \quad i_z = i_p - i_n \quad \text{and} \quad v_w = v_z \]  

(1)

It should be noted from the above expression that the differential input current $i_p - i_n$ is converted to the output voltage $v_z$ through an impedance connected at the port $z$. Thus the CDBA basically consists of two blocks; a current differencing circuit (current subtractor) and a voltage follower. In the following section, we will introduce a low-voltage current differencing circuit providing the difference of the input currents $i_p$ and $i_n$, and a low-voltage buffered voltage amplifier.

![Figure 1 Circuit representation of a CDBA](image)
Low-Input Resistance Input Stage

Fig. 2 shows a low-input resistance input stage, where the transistors Q1-Q4 function as a feedback loop [T. Nagasaku, A. Hyogo, and K. Sekine, 1996]. Assuming that the emitter signal current of Q1 is \( i_e \), the emitter current of Q2 will approximately be equal to \( \beta_2 i_e \). The current mirror formed by Q3-Q4 reflects the current \( \beta_2 i_e \) to the collector current of Q4. Therefore, the input signal current \( i_{in} \) can be expressed as:

\[
i_{in} = i_e + \beta_2 i_e
\]  

(2)

Due to the negative feedback, the input resistance \( r_{in} \) of this circuit is very low and can be given by

\[
r_{in} \approx \frac{r_{e1}}{\beta_2}
\]  

(3)

where \( \beta_2 \) is the current gain of the transistor Q2, \( r_{e1} \) is the small signal emitter resistance which is given by \( r_{e1} = \frac{V_T}{I_{B1}} \) and \( V_T \) is the thermal voltage. Based on the low-input resistance input stage of Fig. 2, in the following section a current subtractor will be developed.

Current Subtractor

The unity gain current amplifier based on the above input stage is shown in Fig. 3. A biasing circuit comprising the transistor Q6 and the bias current source \( I_{m3} \) is added to provide the bias voltage \( V_{B1} \) and the imaginative ground at the input node, while the transistor Q5 and the bias current source \( I_{m4} \) provide the output current \( I_{out} \). Since the relationship between the input signal current \( I_{in} \) and the signal current \( i_e \) can be given by,

\[
i_e = \frac{I_{in}}{\beta_2 + 1}
\]  

(4)

thus, the output signal current \( I_{out} \) of the circuit of Fig. 3 can be expressed as
function as a emitter signal. The current Therefore, the distance which is the input stage.

\[ i_{\text{out}} = -\beta_2 i_e = -\frac{\beta_2}{\beta_2 + 1} i_{\text{in}} \]  

(5)

In general case, the current gain \( \beta_2 \gg 1 \), thus the output current \( i_{\text{out}} \) of this circuit can be written as

\[ i_{\text{out}} \equiv -i_{\text{in}} \]  

(6)

Fig. 3 shows the proposed current subtractor circuit, which is obtained by using two unity gain current amplifiers that are formed by \( Q_1-Q_5 \) and \( Q_7-Q_{11} \). The current mirror \( Q_{12}-Q_{13} \) reflects the current \( i_p \) to the output port, therefore, the output current of this circuit can now be expressed as

\[ i_{\text{out}} = i_p - i_{\text{in}} \]  

(7)
Buffered Voltage Amplifier

The high-input impedance voltage amplifier based on a simple emitter follower is presented in Fig.5, where complementary NPNs and PNP s, Q14-Q17, form an input buffer that forces the w terminal voltage to that of the z terminal. Let us assume that all transistors are well matched and a good matching in $V_{bb}$ between NPN and PNP transistors is obtained in order to achieve low offset voltage. Thus, the input impedance at the port z becomes very high and is approximately equal to

$$r_z \equiv \beta_n \beta_p \left[ \frac{R_e}{2} + R_w \right]$$

(8)

where $\beta_n = \beta_{14} \equiv \beta_{16} >> 1$, $\beta_p = \beta_{15} \equiv \beta_{17} >> 1$, $r_e = r_{e14} = r_{e16} \equiv r_{e15} = r_{e17}$ and $R_w$ is the load resistance connected to the port w. On the other hand, the output impedance at the port w becomes quite low and is equal to

$$r_w \equiv \left[ \frac{R_e}{2} + \frac{R_z}{\beta_n \beta_p} \right]$$

(9)

where $R_z$ is a converting resistor connected to the port z. For example, if $R_e = 1 \, k\Omega$, $R_w = 10 \, k\Omega$, $V_p = 26 \, mV$, $I_{bb} = I_{b3} = 100 \, \mu A$ and $\beta_n \equiv \beta_p = 100$, then $r_e$ and $r_w$ are approximately equal to 10 MΩ and 130 Ω, respectively.

Low-Voltage Current Differencing Buffered Amplifier (CDBA)

The proposed low-voltage CDBA is now shown in Fig.6, which consists of a current subtractor of Fig.4 and a buffered voltage amplifier of Fig.5. All bias current sources of the circuit are realized by current mirror circuits and set to be equal to $I_b$. Since the circuit uses only two transistors and one bias current source between the positive and the negative supply voltages, this circuit can operate at a low power supply voltage of 2 volts (or ±1 volts).
Circuit Performance Analysis

By using a hybrid-π model and a routine small-signal circuit analysis, the performance of the proposed low-voltage CDBA of Fig. 6 can be analyzed as follows. Since the differential input current \( i_{p-n} \) is converted to the output voltage \( v_o \) through the resistance \( R_z \) which is connected at the port \( z \), thus the relationship between the input and output signals of this device can be described in the term of the trans-resistance gain \( R_m \) as

\[
\frac{v_o}{i_{p-n}} = R_m = R_z \left( \frac{1}{1 + \varepsilon_j} \right) \left( \frac{1}{1 + \varepsilon_v} \right)
\]

where \( \varepsilon_j \) is the current transfer error associated with the current subtractor circuit and \( \varepsilon_v \) is the voltage transfer error of the buffered voltage amplifier. Let us assume that \( g_{m1} \) and \( g_m \) denote respectively the transconductance and the small-signal base conductance of the \( i \)-th transistor \( (i = 1, 2, \ldots, 17) \), the current transfer error \( \varepsilon_j \) can be derived as

\[
\varepsilon_j = \left\{ \frac{(g_{mp} + 2g_{xp})}{g_{ma} + g_{pi}} \left[ g_{ma} + 2g_{pi} \left( \frac{1}{1 + \frac{g_{mp}}{g_{ma}}} \right) - g_{mp} g_{ma} \right] }{g_{mp} g_{ma}} \right\}
\]

where \( g_{ma} = g_{n1} = g_{n2} = \ldots = g_{n17} = g_{m1} = g_{m} \), \( g_{ma} = g_{d1} = g_{d2} = \ldots = g_{d17} = g_{d10}; g_{ap} = g_{n13} = g_{n15} = g_{m17}; g_{mp} = g_{d13} = g_{d15} = g_{d17} \) and \( g_{mp} = g_{d13} = g_{d15} = g_{d17} \). For example, if 0.7 \( \mu \)m BiCMOS process parameters are employed under the bias current \( I_B = 100 \mu A \), then we will obtain: \( g_{ma} = 2.23 \times 10^{-3} \text{ A/V}, g_{mp} = 2.14 \times 10^{-5} \text{ A/V}, g_{ma} = 4.17 \times 10^{-5} \text{ A/V} \) and \( g_{mp} = 4.38 \times 10^{-5} \text{ A/V} \). As a result, the transfer error \( \varepsilon_j \) of about 6.12 % is expected.

The second error \( \varepsilon_v \) that is due to the buffered voltage amplifier formed by complementary transistors \( Q_{14} \) to \( Q_{17} \) can be given by
where $G = 1/R_w$. With the same process parameters, the resulting voltage gain error $\varepsilon$, for a load resistance $R_w$ of 10 kΩ is approximately equal to 4.65%.

For the high frequency responses, the high frequency limitation is strongly dependent on the stray capacitances and the current transfer function can approximately be expressed in the relationship of the currents $i_2$ and $(i_0 - i_2)$ by

$$
\frac{v_2}{v_z} = \frac{C_{wI}}{C_{wI} + C_{w2}}
$$

where $C_{wI} = C_{wI} = C_{w2} = \ldots = C_{wI} = C_{w2} = \ldots = C_{wI} = C_{w2}$ and $C_{wI}, C_{w2}$ denote the emitter-base capacitance and the collector-base capacitance of the $i$-th transistor, respectively. The denominator of equation (13) has three poles and can be written as

$$
D_1(s) = \left(1 - \frac{s}{p_1}\right)\left[1 - \frac{s}{p_2 + \frac{1}{p_3}} + \frac{s^2}{p_2 p_3}\right]
$$

where $p_i$ is a pole of equation (13). Usually, the poles $p_2$ and $p_3$ are widely separated. If we assume that $p_3$ is much larger than $p_2$, the term $1/p_3$ can be neglected compared with the term $1/p_2$ in the denominator. Thus, equation (14) becomes approximately

$$
D_1(s) \approx \left(1 - \frac{s}{p_1}\right)\left[1 - \frac{s}{p_2 + \frac{s^2}{p_2 p_3}}\right]
$$

By equating the coefficients in equation (13) with those in equation (15), the pole positions can be obtained as follows

$$
p_1 = \frac{2C_{wI} + 2C_{w2}}{2C_{wI} + C_{w2}}
$$
\[ p_2 = \left[ \frac{g_{mn} + g_{mp}}{2C_{mn} + C_{mp} \left( \frac{g_{mn}}{g_{mn}} \right) + \left( C_{mn} + 2C_{pm} \right) \left( 1 + \frac{2g_{mn}}{g_{mn}} \right)} \right] \]  

(17)

and

\[ p_3 = \left[ \frac{g_{mn}(2C_{mn} + C_{mp}) + (g_{mn} + 2g_{mp})(C_{mn} + 2C_{pm})}{(2C_{mn} + C_{mp})(C_{mn} + 2C_{pm})} \right] \]

(18)

At the port \( w \), the approximate small-signal voltage gain can be written in the term of \( v_w \) and \( v_z \) as

\[ v_w = \frac{\left( g_{mn} + g_{mp} \right) \left( g_{mp} + g_{np} \right)}{(G_w + g_{mp} + g_{np}) \left( g_{mn} + g_{mp} \right) + g_{mp}g_{np}} \]

\[ v_z = \frac{1 + C_{mn} - s}{1 + \left( G_w + g_{mp} + g_{np} \right) C_{mn} \left( g_{mn} + g_{mp} + g_{np} \right)} \]

(19)

The denominator of equation (19) can be rewritten as

\[ D_2(s) = \left[ 1 - s \left( \frac{1}{p_4} + \frac{1}{p_5} \right) + \frac{s^2}{p_4p_5} \right] \neq \left[ 1 - \frac{s}{p_4} + \frac{s^2}{p_4p_5} \right] \]

(20)

where we assumed \( p_4 \ll p_5 \). The poles \( p_4 \) and \( p_5 \) can now be estimated by comparing coefficients in equations (19) and (20). Thus we can identify

\[ p_4 = \frac{\left( G_w + g_{mp} + g_{np} \right) \left( g_{mn} + g_{mn} + g_{mn} \right) + G_w g_{np}}{(G_w + g_{mp} + g_{np}) C_{mn} \left( g_{mn} + g_{mn} + g_{mn} \right) + G_w g_{np}} \]

(21)

and

\[ p_5 = \frac{\left( G_w + g_{mp} + g_{np} \right) + G_w g_{np}}{C_{mn} g_{mn}} \]

(22)

In order to figure the high frequency limitation, let us assume that \( C_{mn} = 8.25 \times 10^{-14} \) F, \( C_{mp} = 8.98 \times 10^{-14} \) F, \( C_{mp} = 4.14 \times 10^{-14} \) F and \( C_{np} = 4.22 \times 10^{-14} \) F. Since the poles \( p_4 \) and \( p_5 \) are the non-dominant poles, the effects of these non-dominant poles are neglected in the calculation. Thus, the poles \( p_4, p_5 \) are approximately located at 1.5 GHz, 2.67 GHz and 2.14 GHz, respectively. Clearly, the high frequency limitation of the circuit is due to the dominant pole \( p_1 \) that is dominated by the transconductance and capacitance associated with the current mirror \( Q_{17}Q_{13} \). However, this dominant pole \( p_1 \) is quite high. Therefore, the circuit can be used in high frequency applications.
Application to Current-Mode Ladder Filters

An approach to derive CDBA-based current-mode ladder filters from passive RLC ladder prototypes will be presented in this section. Due to the low sensitivity nature of doubly terminated RLC ladder filters [R. Schaumann and M.E. Valkenburg, 2001, and P. Huelisman Lawrence, 2000], this configuration has been receiving a considerable attention. These active implementations are conventionally designed based on the representation of signals as voltages. But in the current-mode based implementation, the input, intermediate and output signals are usually represented as electrical currents that seems to be recognized to offer potential advantage for low-voltage applications. To illustrate the design procedure of CDBA-based current-mode ladder filters by the leapfrog, consider a popular ladder structure that realizes the doubly terminated RLC ladder filter shown in Fig. 7. This structure can be characterized by the following expressions

\begin{align}
  i_1 &= i_2 - \frac{v_1}{r_s} - i_2, \quad v_1 = i_1 z_1 \\
  v_2 &= v_1 - v_3, \quad i_2 = v_2 z_2 \\
  v_3 &= i_2 z_3, \quad i_3 = i_2 - i_4 \\
  v_n &= v_{n-1} - v_{n+1}, \quad v_n = v_n z_n \\
  i_n &= i_{n-1} - i_{n+1}, \quad i_n = i_n z_n
\end{align}

(23)

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Using above expressions, a LC ladder filter structure can be represented by the block diagram of the leapfrog realization as shown in Fig. 8. Observe that in this figure the repeated use of two operations of Fig. 9(a) and 9(c) makes up the complete circuit. These operations can easily be realized by the CDBAs as shown in Figs. 9(b) and 9(d). For the CDBA-based filter realization, we can readily obtain the CDBA-RC circuit by interconnecting the corresponding sub-circuits of Figs. 9(b) and 9(d) according to the overall block diagram representation of Fig. 8. As an example of this design procedure, a current-mode fifth-order Butterworth RLC ladder lowpass filter shown in Fig. 10 is realized. The resulting CDBA-based circuit of the filter is shown in Fig. 11, where the normalized cutoff frequency \( \omega_{3dB} = 1 \) rad/s and the values of resistors and capacitors are in \( \Omega \) and \( F \), respectively. It can be seen that five CDBAs are employed for implementation of the fifth-order filter. In general, \( n \)th CDBAs are required for realizing the \( n \)-th-order filters. On the other hand, CCI-l-based implementation in voltage-mode designs of this structure requires some additional devices when they are used for cascading sections due to the high-output impedance [E. El-Masry, 1996. and S. I. Liu, 1991.]. It should be noted that the CDBA-based ladder leapfrog filter implementations can reduce the number of active components by approximately 50% comparing with CCI-l-based [E. El-Masry, 1996. and S. I. Liu, 1991.] and OTA-based [J. Wu and E. El-Masry, 1998. Deliyannis, Y. Sun and J. K. Fidler, 1999. and J. Wu and E. El-Masry, 1998.] filter implementations, and less than 50% when comparing with the realizations using Op-Amps [R. Schaumann and M. E. Valkenburg, 2001. and P. Huelsmann Lawrence, 2000.]

**Figure 9** Sub-circuits and their realizing operation using CDBAs

**Figure 10** Current-mode fifth-order Butterworth RLC ladder lowpass filter
This technique can also be used to design RLC bandpass filters. A sixth-order RLC bandpass filter is shown in Fig. 12, which includes parallel and series resonant circuits as subcircuits. The sub-circuits of the filter are realized by using CDBAs as shown in Fig. 13. Thus the whole structure can be shown in Fig. 14.

Figure 11  CDBA-based realization of the current-mode fifth-order lowpass filter of Fig. 10

\[ V_k = \frac{1}{Z \omega} \left( I_1 - I_2 \right) \]

(a)
Design Examples and Simulation Results

The performances of the proposed low-voltage CDBA of Fig. 6 were confirmed using PSPICE simulation with the 0.7μm BICMOS process parameters. The power supply voltage is ±V = ±1 volts and the bias current is 100 μA. The simulated DC offset current at the port z, for $R_z = 1 \, kΩ$, is very low and is approximately equal to 3.23 μA, and the simulated DC voltage transfer characteristic between the voltages $v_i$ and $v_o$, for $R_o = 10 \, kΩ$, has the DC offset voltage value of about 1.98 mV. The total power consumption was found by the simulation to have a low value of 1.84 mW. Fig. 15 shows the simulated frequency responses of the current and voltage transfer characteristics of the proposed CDBA. It is clearly seen from the figures that the bandwidth frequencies in the range of hundred MHz are obtained. The simulation results show that the circuit has a wide bandwidth and low-power consumption.
As an illustration of a current-mode fifth-order Butterworth lowpass filter, the filter of Fig. 10 with a -3dB frequency \( \omega_{-3dB} \) of 100 Mrad/s was designed. This condition leads to the passive element values as follows: \( R_s = R_1 = R = 1 \) k\( \Omega \), \( C_1 = C_2 = 6.18 \) pF, \( L_2 = L_4 = 16.18 \) pF, and \( C_3 = 20 \) pF. The simulated and theoretical responses are shown in Fig. 16.

**Figure 15** Simulated frequency responses of the proposed CDBA
the filter of leads to the 16.18 pF, and

Figure 16 Simulated responses for the fifth-order Butterworth low pass filter of Fig. 11

Figure 17 Simulated responses for the sixth-order Chebyshev bandpass filter of Fig. 14
For illustrative purposes, a sixth-order Chebyshev bandpass filter was also designed with the following specifications; \( \omega_{sdb} = 100 \text{ Mrad/s} \), bandwidth (BW) = 0.45, and passband ripple = 0.1 dB. These specifications resulted in the following component values; \( R_s = R = 1 \text{ k}\Omega, C_1 = C_2 = 22.923 \text{ pF}, C_3 = 3.921 \text{ pF}, L_1 = L_2 = 4.362 \text{ pF}, \) and \( L_3 = 25.498 \text{ pF} \). The simulated responses of the designed filter together with the theoretical values are shown in Fig. 17.

Conclusions

A design technique for realizing the low-voltage current differencing buffered amplifier (CDBA) and its application to implement continuous-time current-mode leapfrog ladder filters has been described. The proposed circuit can operate at a low power supply voltage as well as high-frequency operations, and can easily be implemented in a monolithic integrated circuit. The simulated responses with PSPICE are quite good over a wide frequency range and the circuit requires low-power consumption. As seen from applications, we prove that it is very suitable for realizing any current-mode leapfrog ladder filters employing CDBAs as an active element. The proposed technique requires \( n \)-CDBAs for the realization \( n \)-order ladder filter, which is a significant active element reduction in comparison with the previously reported methods using Op-amps, OTAs, and CCIIs.

Acknowledgment

This work is partly supported by the Thailand Research Fund (TRF) under the Senior Research Scholar Program, grant number RTA4680003.

References