EASR

Engineering and Applied Science Research

https://www.tci-thaijo.org/index.php/easr/index

Published by the Faculty of Engineering, Khon Kaen University, Thailand

Electrostatic Discharge (ESD) and Electrical Overstress (EOS): The state of the art in components to systems

Steven H. Voldman*

IEEE Fellow, Lake Placid, New York, 12946, USA.

Received April 2016
Accepted June 2016

Abstract

Electrostatic Discharge (ESD), Electrical Overstress (EOS) and electromagnetic compatibility (EMC) continue to impact semiconductor manufacturing, semiconductor components and systems as technologies scale from micro- to nano-electronics. The range of concern for components include semiconductor components, magnetic recording industry, MEMs, and for products from disk drives, cell phones, notebooks, tablets, laptops, and desktop computers. The objective of this lecture is to address the state of the art of electrostatic discharge (ESD) and electrical overstress (EOS) in today's electronic components and systems. The tutorial provides a clear picture of ESD, EOS and EMC phenomena, sources, physics, failure mechanisms, testing and qualification of components and systems. The conclusion of this talk is that ESD and EOS continue to be a concern in technologies from micro-electronics to nano-structures, and will remain a reliability and quality issue in the future.

Keywords: Electrostatic discharge, Electrical overstress, Electromagnetic compatibility, Electrical over-voltage, Electrical over-current

1. Introduction

Electrostatic discharge (ESD) and electrical overstress (EOS) have been an issue in both electronic components and electrical systems with the introduction of integrated circuits and a focus on quality and reliability [1]. In the mid-1970's, it was apparent that significant work on ESD and EOS was required to provide reliable semiconductor components. The work required included physical understanding of the failure mechanisms of semiconductor components, circuit protection devices, and standard development. In the area of circuit protection devices, solutions were required to understand the desired electrical characteristics at high current and high voltage, the circuit topology, as well as physical layout. In this time frame, there were few technical publications, few patents, no books, no ESD standards, and no commercial test equipment. ESD learning occurred within corporations, and military institutions, but information was held as confidential.

In 1979, with the initiation of the Electrostatic Discharge Association (ESDA), publications of electrostatic discharge (ESD) and electrical overstress (EOS) were released to the public domain. In these early publications, the ESD and EOS failure mechanisms, circuits and standards were being discussed. Additionally, publications were also present in the International Reliability Physics Symposium (IRPS), which noted that ESD and EOS was a reliability concern in semiconductors. Today, there are still concerns with ESD, EOS, latchup, electromagnetic interference (EMI), and electromagnetic compatibility (EMC) (Figure 1).

In this publication, the state of the art of ESD and EOS will be discussed. The discussion will include semiconductor failure mechanisms, semiconductor circuit design, design layout techniques, testing methods, and standards. The topics will address both ESD and EOS in components of systems [1-10].

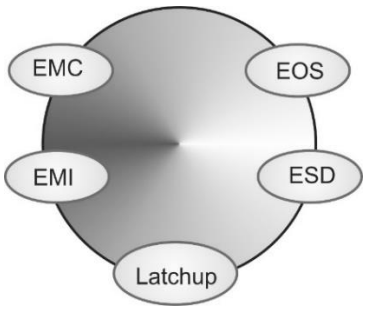

Figure 1 ESD, EOS, Latchup, EMI and EMC

2. Electrostatic Discharge (ESD) and Electrical Overstress (EOS)

2.1 ESD failure mechanisms

ESD failures are a function of both the semiconductor device, and the type of ESD stress test. Each waveform applies a different type of stress to a semiconductor device

*Corresponding author. Tel.: +1-802-922-1447
Email address: voldman@ieee.org
doi: 10.14456/easr.2017.18

or circuit [2-3]. In semiconductor devices, ESD failure can occur in the semiconductor, dielectrics, and conductors [3]. Semiconductors exist as a substrate wafer and are intrinsic, p-type or n-type. Dielectric failure can occur in the gate dielectric in the MOSFET, isolation regions, or inter-level dielectric (ILD) used in the back end of line (BEOL) materials. In silicon on insulator (SOI) technology, the buried oxide (BOX) layer can fail from ESD stress events. The metal interconnects, which consists of the contacts, vias, and conductor films used in wiring, or in inductors can fail from ESD events. In the cases of silicon regions or metal conductors, if the melting temperature of the materials is exceeded, damage can occur in the device. In dielectrics, if the breakdown voltage is exceeded, dielectric failure occurs [2-3].

ESD failure can occur when the power-to-failure is exceeded. The power-to-failure is a function of the material properties such as the adiabatic, thermal diffusion time, and steady state thermal characteristics. As a result, ESD failure is a function of the pulse width applied to the component. The dependency of power-to-failure versus pulse width is known as the Wunsch-Bell plot [2-3].

2.1.1 Human Body Model (HBM)

From human body model (HBM) ESD events, the ESD pulse is applied to the signal pads and the power pads. ESD failure occurs in both the peripheral circuits and the ESD networks. The HBM pulse is either a positive or negative polarity event having a pulse width associated with a fixed RC time. On the peripheral circuits, the ESD networks can consist of diodes, or MOSFETs that are normally off during chip operation or a powered state. Failures can occur in the CMOS active or passive elements. Current is transferred to the power or ground rail, to avoid failure of the sensitive circuits on the signal pads. Unique circuits, that respond to the RC pulse (e.g., RC-triggered power clamps) to transfer current to the grounded reference during an ESD event.

With scaling technology, the challenge is how to protect the sensitive circuits as they are reduced in the layout area. Additionally, the ESD networks must also be reduced in loading capacitance to meet the performance objectives of the semiconductor chip. Hence, as technology migrates to future generations, the difficulty is to provide smaller and more robust ESD networks to maintain the quality and reliability of the semiconductor chip. As a result, the challenge remains as products are scaled to nano-technology [2, 10].

2.1.2 Machine Model (MM)

A second ESD model is the machine model (MM) event. The MM event is faster and has a higher current than the HBM event, with a significantly faster rise time and current magnitude. This event is also applied to the peripheral bond pads, Due to the oscillatory nature of this event, the ESD circuitry must address both positive and negative events. As semiconductor chips are scaled, it is more difficult to address the ESD current from MM events [2, 10].

2.1.3 Charged Device Model (CDM)

A third model, known as the charged device model (CDM), addresses the charging of the component substrate or power grid to a fixed voltage, and then discharged through the signal pins. The amount of charge stored is a function of the component size. Additionally, the event is a fast event, in the nanosecond time regime. Unique failures occur as the current flows from the charged core to the periphery of the grounded signal pin. ESD networks are designed to avoid current flow through dielectrics and allow discharge through desired paths [2, 10]. Figure 2 shows an example of a CDM MOSFET gate failure in a receiver network.

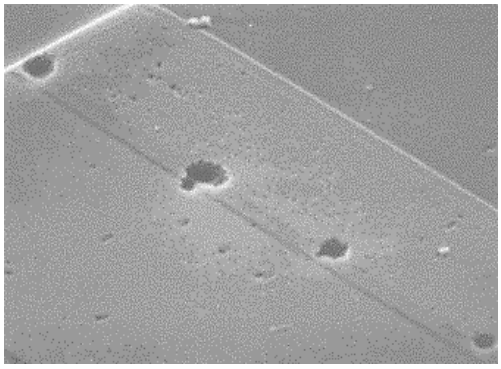

Figure 2 Charged device model (CDM) failure in a MOSFET gate region

2.2 ESD circuits

In the following section, a brief view of ESD circuits are highlighted in digital, analog and RF applications [5-9].

2.2.1 Digital circuits

ESD networks for digital circuits are typically dual-diode networks, or grounded gate MOSFET networks. To avoid failure of the digital circuits, series resistors are placed between the ESD networks and the I/O circuits. To address CDM events, resistors are placed between a primary dual-diode network, and a secondary dual-diode network that is placed adjacent to the receiver networks [5-6].

2.2.2 Analog circuits

ESD networks for analog circuits have a different layout and architecture compared to digital circuits [6-7]. Differential receivers in analog applications require highly matched ESD networks, as well as an additional network between the two input signals of a differential receiver. This is achieved using common centroid layout techniques. Additionally, in digital-analog mixed signal applications, failures can occur as signal is passed from the digital to analog core regions. Power domains of digital and analog components are separated for noise, with the consequence of introducing ESD issues core-to-core. Unique ESD networks are placed internal to the semiconductor chip between the signal lines that pass between the digital core and the analog core, as well as networks to interconnect the ground rails.

2.2.3 Radio Frequency (RF) circuits

ESD networks for radio frequency (RF) applications are significantly different from other networks since circuit architecture is addressed in the frequency regime [9]. In RF applications, RF design techniques are used for ESD networks. An ideal RF ESD network has zero impedance in the "ESD time regime" and infinite impedance in "RF application regime." Diode elements and MOSFETs do not provide this type of frequency domain characteristics, but inductors do have this property. Secondly, digital and analog

ESD solutions incorporate resistor elements for ballasting and buffering of ESD currents. From an RF perspective, resistors elements generate noise and are undesirable in their frequency domain characteristics. As a result, inductor-diode and inductor-MOSFET concepts exist. Additionally, RF circuitry is significantly different, utilizing bipolar junction transistors (BJT), hetero-junction bipolar transistors (HBT) and RF MOSFETs.

For noise isolation, the power domains of the digital, analog and RF cores are separated. From an RF perspective, RF coupling of the domains hampers RF circuit stability and other RF parameters. Hence, there is a tradeoff between ESD robustness and RF coupling between the power domains [6-9].

2.3 ESD design discipline

The ESD design discipline is distinct from circuit design, utilizing many different concepts normally not practiced by circuit designers. Additionally, ESD design layout for digital, analog and RF design incorporate different techniques that are best suited for ESD protection and the application design style.

ESD digital design practice incorporates the following [5]:

- Device Response to External Events - ESD circuit respond to the ESD pulse events
- Alternate Current Loops - Establishment of current paths through the power grid to avoid the devices in the signal path
- Switches – devices that turn on during an ESD event to allow current through the alternate current loop
- Decoupling of Current Paths - decoupling of the current flow through the signal path
- Decoupling of Feedback Loops – decoupling of feedback loops that lead to failure
- Decoupling of Power Rails – decoupling of power rails that contain sensitive circuitry
- Local and Global Distribution – distribution of the current through parallel elements and paths to reduce the current in any given circuit element
- Use of parasitic elements for ESD solutions
- Buffering - preventing current flow through a given path using resistors, inductors or other elements
- Ballasting - a technique to distribute current through parallel elements
- Unused Sections of a Semiconductor Device, Circuit or Chip Function - using circuitry for ESD that is not being used for a functional purpose
- Impedance Matching between Floating and Non-Floating Networks - matching of elements to current flows evenly through different parallel networks
- Unconnected Structures - use of structures that are not being utilized for functional operation
- Utilization of “Dummy Structures” and Dummy Circuits - use of circuits to provide improved impedance matching and improved distribution of current

ESD analog design practice additionally incorporates the following [7]:

- Common Centroid Design - design layout to prevent mismatch in ESD circuits and I/O
- Corner Utilization for ESD Power Clamps – placement of ESD power clamps in regions where it is not desirable or restricted from use for analog circuits
- Digital VSS-to-Analog VSS ESD Networks - ESD networks placed between the ground connections to allow a current path between all pin-to-pin and pin-to-rail combinations
- Signal Path Internal ESD Networks - placement of ESD elements on signal lines between drive circuits of a digital core, and the receivers of an analog core

ESD RF design practice additionally incorporates the following [9]:

- Frequency Domain ESD - ESD elements that have no impedance below the operational function range of an RF network, and infinite impedance during RF operation
- Inductor Utilization - use of inductors to utilize low impedance at low frequency and infinite impedance at high frequency
- LC Tank Resonance - use of the resonant frequency of an LC tank matched to the functional application frequency for ESD networks
- Narrow Band ESD Circuits - a signal tuned frequency ESD for narrow band circuits
- Broadband ESD Circuits - a multi-stage ESD network that utilizes distribution techniques to lower impedance at low frequencies
- Inductive Isolation - use of inductors to isolate circuitry
- Component Substitution - replacement of passive capacitors for conducting circuit elements (e.g., diodes)
- Robust RF Passive Elements - RF passives customized for improved ESD protection

2.4 ESD testing

ESD testing to simulate ESD events, and evaluate the ESD robustness of components and systems for quantification of the reliability and quality is a critical part of the ESD discipline [10]. Today, there is commercial test equipment available to evaluate many types of ESD phenomena (Figure 3).

Figure 3 Commercial wafer level ESD test system

2.4.1 Human body model

Human body model (HBM) testing continues to evolve due to today’s complexity, test time, and matrix issues. One

of the key changes is the focus on the pin combinations. Continued problems with the switching matrix between the pins are leading to questions to whether it should be simplified. HBM testing may evolve into a simple two pin test without the complexity of today's specifications [10].

2.4.2 Transmission Line Pulse (TLP)

Transmission line pulse (TLP) testing evaluates the responsiveness of a device, ESD networks and circuits to a pulse event with a fixed rise time and fixed fall time [10]. TLP measurements apply a 100ns pulse to a device under test (DUT). TLP measurements provide a TLP I-V characteristic of the DUT highlighting the trigger voltage, the holding voltage, the pulsed series on-resistance and the second breakdown current. The pulse width is chosen to mimic an HBM event energy equivalency. This was developed into a standard practice after the year 2000. Today, commercial test systems exist using this method.

2.4.3 Very Fast Transmission Line Pulse (VF-TLP)

Very fast transmission line pulse (VF-TLP) testing evaluates the responsiveness of a device, ESD networks, and circuits to a faster pulse event with a fixed rise time and fixed fall time [10]. VF-TLP measurements apply a 10ns pulse to a device under test (DUT). Like the TLP measurement, the VF-TLP measurements provide a VF-TLP I-V characteristic of the DUT highlighting the trigger voltage, the holding voltage, the pulsed series on-resistance and the second breakdown current. Standardization of this method was completed after the TLP standard practice (i.e., after the year 2000). Commercial equipment also exists to apply this method.

2.4.4 Human Metal Model (HMM)

The human metal model (HMM) is a new standard to address the use of a system-level waveform on a component [10]. The HMM standard uses the IEC 61000-4-2 standard pulse event with a high current fast peak. The uniqueness of this HMM standard is that only the pins that are ports of the external system are required to be tested. In this test, only the direct contact discharge is required. This standard was initiated by pressure from system developers to address the issue that the components failed in the systems when the IEC 61000-4-2 pulse was applied. System developers wanted to have the component survive a system-like test.

2.5 Electrical Overstress (EOS)

In recent years, there has been a resurgence of interest in electrical overstress (EOS) [4]. One of the reason is that it still remains the dominant cause of field failures. Secondly, significant advancements were made in ESD, yet the advancement of the state of the art for EOS has been not been as significant. For the next ten years, there will be continued focus on EOS in components and systems.

2.5.1 Electrical Overstress (EOS) failure mechanisms

Electrical overstress (EOS) failures include failures in the component and in the system [10]. Figure 4 is a plot showing the range of sources that cause electrical overstress. The EOS sources can range from exceeding the safe operating area (SOA), product mismatch, to printed circuit board (PCB) design issues.

Component level EOS failures include those involving packaging material, packing leads, wire bonds, and on-silicon failures. On the printed circuit board (PCB), EOS failures can include PCB traces, PCB insulator films, and EOS protection elements.

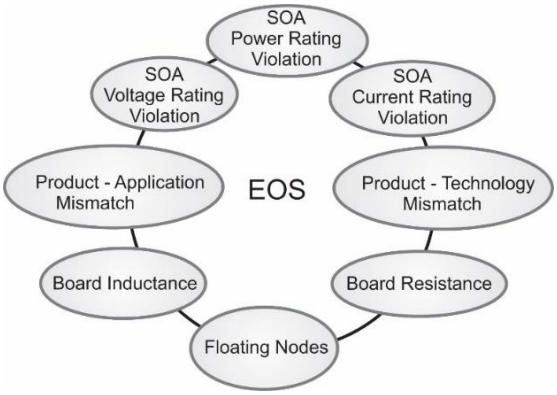

Figure 4 Electrical overstress (EOS) sources

2.5.2 EOS circuits

EOS protection circuits can exist on-chip or on-board. EOS protection elements can be single direction or bi-directional. EOS protection elements can include Zener diodes, Schottky diodes, metal oxide varistors (MOV), resistors, fuse elements, anti-fuses, gas discharge tubes (GDT), to electrical circuit breakers. EOS protection elements can serve as a first stage of electrical protection to limit the current flowing into the component [10].

2.5.3 EOS system level testing

2.5.3.1 Wunsch Bell power-to-failure plot generation

For evaluation of the EOS robustness, the Wunsch-Bell plot can be generated by applying various pulse widths from the adiabatic time scale to the steady state time scale [1-3, 10]. The EOS regime will extend from the time regime of 500ns to seconds. With the generation of the Wunsch-Bell plot, a universal power-to-failure plot is formed for the device, or circuit.

2.5.3.2 Long Duration Transmission Line Pulse (LD-TLP)

Long duration transmission line pulse (LD-TLP) testing evaluates the responsiveness of a device, ESD networks and circuits to a longer pulse event of interest to electrical overstress (EOS) development, research, and qualification [10]. LD-TLP measurements apply a 500ns pulse event to the device under test (DUT). Today, this method is neither a standard practice nor a standard test method. It is anticipated that standardization of the LD-TLP event will occur by 2020.

2.5.3.3 IEC 61000-4-2

System level testing utilizes a high current ESD gun that provides a specific pulse waveform [1, 10]. The established standard used for system level testing is known as the IEC

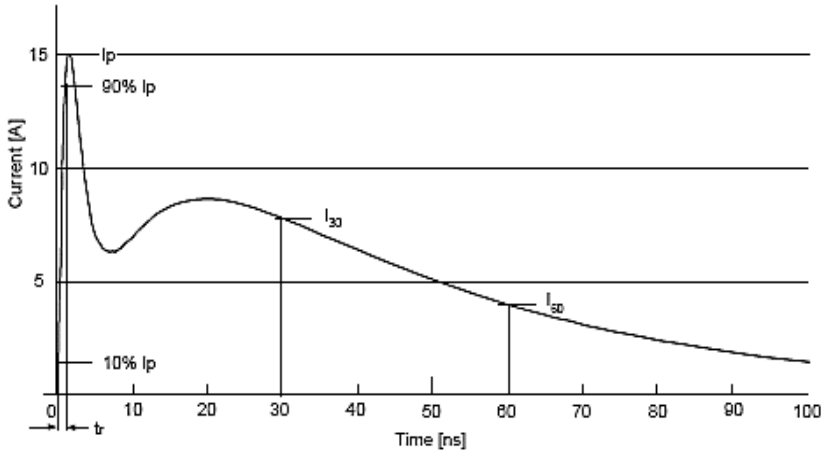

Figure 5 IEC 61000-4-2 pulse waveform

61000-4-2 standard. This test can be provided as a direct contact or air discharge. The charge from the tip of the ESD gun provides a high current fast pulse, followed by a slower RC- HBM like event. The RC characteristic is due to the capacitor-resistor network contained within the ESD gun (Figure 5).

2.5.3.4 IEC 61000-4-5

System level testing for surge events is also important. An established standard used for transient surge system level testing is known as the IEC 61000-4-5 standard [1, 10]. This test provides an understanding of the response to such an event.

2.5.3.5 Cable Discharge Event (CDE)

Cables can lead to electrical overstress of systems. Cables act as charged transmission lines that can inject a pulse into a system. A cable discharge event (CDE) test method has been established [10]. This has been an issue in large computer systems for many years, but never established as a standard until recently. The growth of long UTP CAT5 and CAT6 cables in networks has lead to increased concern in recent years. Commercial test equipment exists for quantification and standardization of this testing.

2.5.3.6 Latchup

Latchup is a form of electrical overstress (EOS) associated with initiation of parasitic pnpn structures within a CMOS semiconductor chip (Figure 6). Latchup failure occurs when a parasitic pnpn device is initiated by regenerative feedback, and the circuit undergoes a high current/low voltage state, followed by thermal breakdown. Latchup can be addressed by both design layout (i.e., spacing of critical dimensions) and semiconductor process solutions [11].

As technologies advance, the critical spacing is decreased, and the substrate resistance is increased. Reduction of the spacing between a PFET and an NFET devices leads to increased parasitic bipolar current gain, leading to a higher regenerative feedback between the parasitic pnp and npn. A lowering of the substrate doping concentration leads to increased shunt resistance, lowering the latchup robustness of the npn transistor (allowing the transistor to undergo a forward active state). A semiconductor process solution to prevent latchup with CMOS technology scaling is the use of a buried guard ring (BGR) structure consisting of a heavily doped buried layer (HDBL) and low resistance shunt. This structure lowers the parasitic bipolar current gain, as well as lowering the substrate resistance shunt.

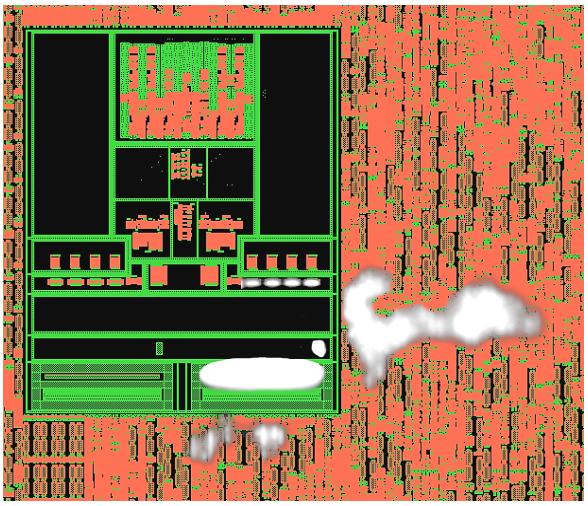

Figure 6 Latchup propagation in a semiconductor chip

2.5.4 EOS design

2.5.4.1 Component level design

Component EOS design practices include on-chip EOS protection elements, EOS-ESD co-synthesized circuits, as well as interconnect wiring that can avoid failure during EOS events. This can include wider wiring connections from bond pad-to-protection network, and expanded width of the power and ground interconnections.

2.5.4.2 Printed Circuit Board (PCB) design

Printed circuit board (PCB) design practices can be integrated into the printed circuit board for mitigating and minimizing electrical overstress (EOS) implications. This can be achieved by both design of PCB ground planes and traces, as well as PCB component placement [4, 10]

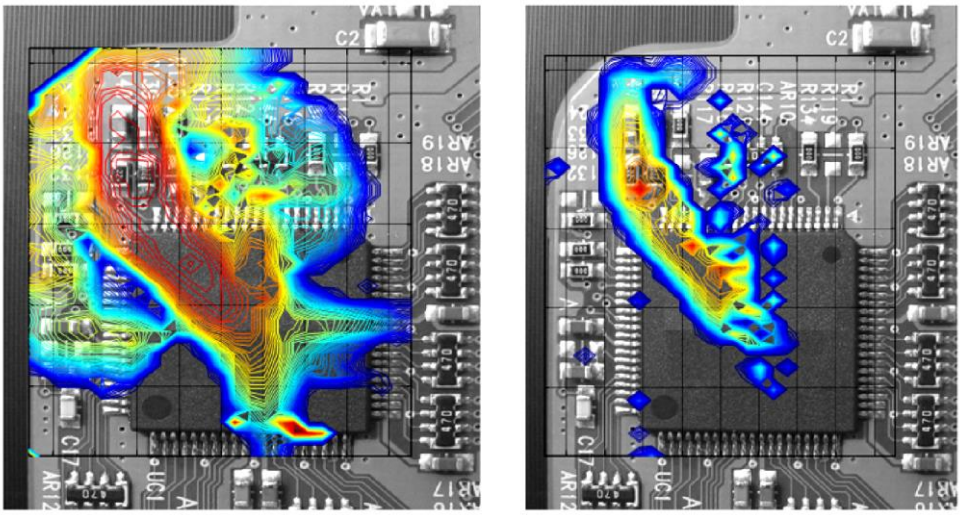

Figure 7 ESD-EMC sensitivity of scanning method comparison of two products

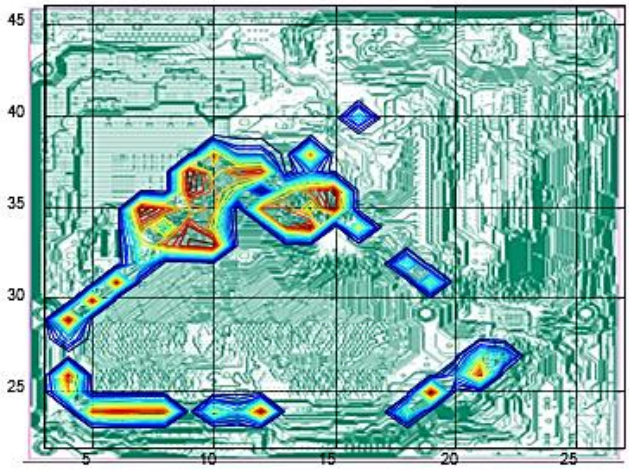

Figure 8 ESD-EMC scan of a printed circuit board (PCB) highlighting sensitivity to electromagnetic interference (EMI)

2.5.4.3 EOS-ESD Co-design

Historically, ESD development was performed on components, and EOS development applied to systems were evaluated independently. Recently it was acknowledged that components can lead to system failures and ESD solutions can lead to EOS system level failures. As a result, there is a growing interest in EOS-ESD co-design of the component ESD strategy, as well as the EOS system level strategy [4, 12].

2.5.4.4 ESD-EMC scanning methodologies

Understanding of the effect of electromagnetic noise on systems and determining the regions of sensitivity was historically difficult. New scanning methods have been developed for product development to determine the regions of sensitivity in components and populated printed circuit boards. Figure 7 shows a comparison of two products mounted on the same printed circuit board. A local EM pulse is placed over the populated printed circuit board to evaluate the system disturbance.

Evaluation of EMC issues in printed circuit boards can be done by visualizing the locations where EMI can enter the system. In the design of printed circuit boards, the ground planes between analog and digital domains can lead to locations where noise can penetrate into the system. Figure 8 is an example of an EMC scan of a printed circuit board, highlighting the locations of noise entry into the system.

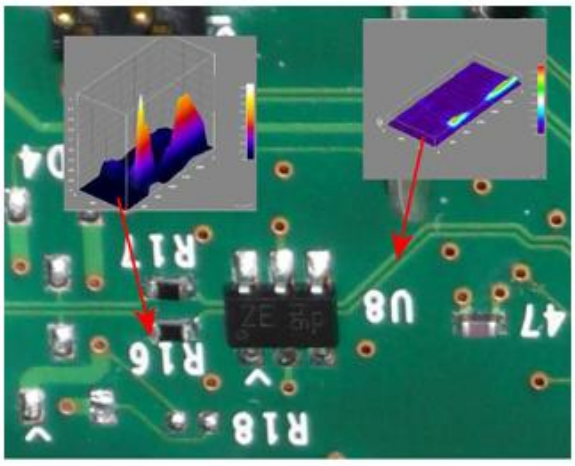

Figure 9 Current reconstruction electromagnetic signal scanning technique

2.5.4.5 Current reconstruction methodology

A second method is to inject an ESD current pulse into the signal lines, and measure the EM signal. Using the scanning armature, EM signal propagation from the ESD event is measured locally across the product. Figure 9 shows the signal entering before the protection resistor elements, as well as measurement of the residual current flowing through the system. By measurement of the electromagnetic signal with the scanning armature, one can determine the incoming current, and how it propagates through the system. These are significant advancements in understanding the effectiveness of protection networks, and how they function within a system. This new method allows for co-design of ESD networks, and systems for evaluation of ESD, EOS, EMI and EMC.

3. Results

Research and development of electrostatic discharge (ESD) phenomena has been significant since the late 1970's leading to advancement of the quality and reliability of components. Advancements in the area of physical understanding, physical design and layout, ESD circuit topology and design, standard development, chip architecture and testing has led to continuous improvement of ESD protection levels in digital, analog, RF application. However, with technology scaling and today's performance objectives, ESD protection levels and reliability have been decreasing.

In the area of electrical overstress (EOS), continued progress is needed to improve the reliability of components and systems in the future. Significant work will be required for the next 10 to 20 years to provide EOS robust systems.

4. Discussion

Continued research will be required for both ESD and EOS in the area of protection circuits, layout and design, testing, and standards development. To make progress on reliability and quality, continued standard development on future application spaces will be required for cell phones, magnetic recording, memory products, to the Internet of Things (IoT) to keep pace with the demands of the future. Standards are needed for charged board model (CBM), long duration TLP (LD-TLP), to ultra-fast TLP (UF-TLP).

5. Conclusions

Continued work will be required for future technology to provide ESD and EOS robust components and systems. In the area of electrical overstress (EOS), there is still a significant amount of research and development required for future components and systems for nano-technologies.

6. Acknowledgements

The author would like to thank the KKU technical program committee for its invitation to provide an Invited Talk at the 6th KKU International Engineering Conference 2016. A special thank you to General Chair Professor Jo Chiranut Sa-ngiamsak of KKU, and Dean of the Faculty of Engineering, Apirat Siritaratiwat, of KKU.

7. References

[1] Voldman S. ESD basics: from semiconductor manufacturing to product use. Chichester, UK: John Wiley and Sons Ltd.; 2012.
[2] Voldman S. ESD: physics and devices. Chichester, UK: John Wiley and Sons Ltd.; 2004.
[3] Voldman S. ESD: failure mechanisms and models. Chichester, UK: John Wiley and Sons, Ltd.; 2009.
[4] Voldman S. Electrical Overstress (EOS): Devices, circuits, and systems. Chichester, UK: John Wiley and Sons, Ltd.; 2013.
[5] Voldman S. ESD: circuits and devices. Chichester, UK: John Wiley and Sons, Ltd.; 2005.
[6] Voldman S. ESD: circuits and devices. 2nd Ed. Chichester, UK: John Wiley and Sons, Ltd.; 2015.
[7] Voldman S. ESD: analog circuits and design. Chichester, UK: John Wiley and Sons, Ltd., 2014.
[8] Voldman S. ESD: design and synthesis. Chichester, UK: John Wiley and Sons, Ltd.; 2011.
[9] Voldman S. ESD: RF circuits and technology. Chichester, UK: John Wiley and Sons, Ltd.; 2006.
[10] Voldman S. ESD testing: from components to systems. Chichester, UK: John Wiley and Sons, Ltd., 2016.
[11] Voldman S. Latchup. Chichester, UK: John Wiley and Sons, Ltd.; 2007.
[12] Duvvury C, Gossner H. System level ESD co-design. Chichester, UK: John Wiley and Sons, Ltd. 2015.